LISTING OF CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application:

Claims

1. (Previously Presented) A computer system including:

a processor;

a first controller;

a random access memory having a plurality of locations for volatile storage of data; and

a data communications facility interconnecting said processor, said first controller, and said random access memory;

wherein said first controller is responsive to a command received from the processor to commence transmission of a quantity of data from a first random access memory location to a second random access memory location, wherein said command specifies said first and second random access memory locations, with the first controller monitoring operation of the processor to terminate the transmission of the data to the second random access memory location, during transmission of the quantity thereto, in response to the processor generating a write request to the second random memory location.

2. (Previously Presented) The system of claim 1, wherein said random access memory is coupled to said data communications facility via a memory controller, said memory controller configured manage operations for said random access memory.

3. (Previously Presented) The system of claim 2, wherein the data is copied from the first random access memory location to the second random access memory location by an internal memory transfer, without traveling over the data communications facility.

4. (Previously Presented) The system of claim 2, wherein said first controller is provided by said memory controller.

5. (Previously Presented) The system of claim 1, wherein a first portion of the random access memory is coupled to said data communications facility via a first memory controller and includes said first random access memory location, and a second portion of random access memory is coupled to said data communications facility via a second memory controller and includes said second random access memory location.

6. Canceled

7. Canceled

8. Canceled

9. Canceled

10. (Previously Presented) The system of claim 1, wherein the processor continues processing operations prior to data being completely copied to the second random access memory location .

11. (Currently Amended) The system of claim 10, wherein the first controller redirects a read request for the second random access memory location to the first random access memory location ~~if the copy has not yet completed~~ during processing of said command.

12. (Currently Amended) The system of claim 10, wherein the first controller delays a write request for the first random access memory location pending completion of the **[[copy]]** command.

13. Canceled

14. (Previously Presented) The system of claim 1, further comprising a cache, and wherein any cache entry for the second random access memory location is invalidated in response to said command.

15. Cancelled

16. (Previously Presented) The system of claim 14, wherein any updated cache entry for the first memory random access location is flushed to memory in response to said command.

17. (Previously Presented) The system of claim 1, wherein said processor supports a specific programming command to copy data from a first random access memory location to a second random access memory location.

18. Cancelled

19. Cancelled

20. (Previously Presented) The system of claim 1, wherein said first controller transmits an acknowledgement of said command back to the processor, and wherein the processor is responsive to a failure to receive said acknowledgement within a predetermined time-out period to perform said copy operation by issuing separate read and write commands.

21. (Canceled)

22. (Currently Amended) A method for operating a computer system including a processor, a first controller, a random access memory having a plurality of locations for volatile storage of data, and a data communications facility interconnecting said processor, said first controller, and said random access memory, said method comprising:

issuing a command from the processor to the first controller, said command specifying a first random access memory location, of said plurality of locations for volatile storage of data, and a second random access memory location of said plurality of locations for volatile storage of data; and

responsive to receipt of said command by the first controller, commencing transmission of a quantity of data from the first random access memory location to the second random access memory location; and

terminating the transmission of the data to the second random access memory location, during transmission of the quantity thereto, in response to the processor generating a write request to the second random memory location.

23. Cancelled

24. (Previously Presented) The method of claim 22, wherein the data is copied from the first random access memory location to the second random access memory location by an internal memory transfer, without traveling over the data communications facility.

25. (Previously Presented) The method of claim 22, wherein the processor continues processing operations prior to data being completely copied to the second random access memory location .

26. (Currently Amended) The method of claim 25, further comprising redirecting a read request for the second random access memory location to the first random access memory location ~~if the copy has not yet completed~~ during processing of said command.

27. (Currently Amended) The method of claim 25, further comprising delaying a write request for the first random access memory location pending completion of the **[[copy]]** command.

28. Canceled

29. (Previously Presented) The method of claim 22, wherein the computer system further comprises a cache, and wherein said method further comprises invalidating any cache entry for the second random access memory location in response to said command.

30. Cancelled

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31. (New) A computer system including:

a processor;

a controller;

a data communications facility interconnecting said processor and controller; and

a volatile storage device having a plurality of locations for volatile storage of data, said controller being responsive to a command received from the processor to copy data from a first of said plurality of memory locations to a second of said plurality of memory location, responsive to memory access requests from said processor to determine a delay in access by said processor to one of said first and second memory locations, with said delay being dependent upon a type of said request and the location among said first and second memory locations to which said access is directed.

32. (New) The system as recited in claim 31 wherein a first portion of said volatile storage device coupled to a data communications facility via said controller and includes said first memory location, and a second portion of memory is coupled to said data communications facility via an additional memory controller and includes said second memory location.

33. (New) The system as recited in claim 33 wherein the data is copied from said first memory location to said second memory location by using a peer-to-peer copy operation on the data communication facility.

34. (New) The system as recited in claim 34 wherein said data communications facility supports direct memory access (DMA), and said peer-to-peer copy operation is performed by using a transaction analogous to DMA.

35. (New) The system as recited in claim 31 wherein the controller maintains a record of copy operations that are currently in progress.

36. (New) The system as recited in claim 31 wherein said request is a read request for said second memory location and the controller redirects said read request to facilitate reading data from said first memory location during processing of said command.

37. (New) The system as recited in claim 31 wherein said request is write request directed to said first memory location and said controller delays said write request pending completion of said command.

38. (New) The system as recited in claim 31 wherein transmission of a quantity of data from a said first memory location to said second memory location occurs in response to said command and said request is a write request directed to said second memory location with said controller being responsive to said write request to terminate said transmission of said data to the second random access memory location, during transmission of the quantity thereto, in response to said write request.

39. (New) The system as recited in claim 31 wherein said controller transmits an acknowledgement of said single command back to the processor, and wherein the processor is responsive to a failure to receive said acknowledgement within a predetermined time-out period to perform said copy operation by issuing separate read and write commands.